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IMPROVED METHOD FOR PRODUCING LOW/HIGH VOLTAGE THRESHOLD TRANSISTORS IN SEMICONDUCTOR PROCESSING

BACKGROUND OF THE INVENTION

[0001] The present invention relates generally to semiconductor processing and, more particularly, to a method for improving the process of forming low and high voltage threshold transistors on semiconductor wafers.

[0002] In the semiconductor device manufacturing industry, efforts are continuing for the purpose of further downsizing a single package semiconductor device. The initial efforts in the miniaturization of a semiconductor device were directed to reduce the size of the semiconductor chip itself. By making the semiconductor chip smaller, the number of chips that could be obtained from one wafer was increased. In addition to bringing down manufacturing costs, the operating speed was increased since the movement distance of electrons between each element could be made shorter. Further, the development of microscopic processing technology decreased the chip size and allowed for the manufacture of a semiconductor device having the same functions. The current leading-edge design guideline for a device is less than 0.18 mu., and thus, it has become possible to place more than two million units on a single semiconductor chip.

[0003] As the size of the semiconductor device decreases, electric current from leakage gets more important. Leakage current limits the performance of the semiconductor device. Libraries with high voltage threshold (vt) transistors run at slower speeds but leak less power when they are inactive. Low vt cells, however, run faster but create more leakage current. Semiconductor device designers are constantly trying to find the right mix of low and high vt transistors in the

device to optimize its performance. In addition, any reduction in processing steps usually means that the cost of making each device is cheaper and is highly desirable.

[0004] Therefore, what is needed, is a system and method that provides any savings of the cost in producing semiconductor devices. Further, optimization of the design of semiconductor devices is also needed.

SUMMARY OF THE INVENTION

[0005] The present invention provides a reduction in mask layers in producing low and high vt transistors. Moreover, the present invention also provides a method of optimizing the speed of the transistors.

[0006] The present invention provides a system and method for processing low voltage threshold transistors on a semiconductor wafer. The method may include: forming core transistors with drains on the semiconductor wafer; forming low voltage threshold transistors with drains on the semiconductor wafer; forming input output transistors with drains on the semiconductor wafer; forming a spacing layer over the core, low voltage and input output transistors; forming a first photoresist mask layer over the low voltage transistors; doping the drains of the core and the input output transistors, wherein the doping is a medium doping; forming a second photoresist mask layer over the input output transistors; and doping the drains of the core and the low voltage threshold transistors, wherein the doping is a medium doping.

[0007] A second method of the invention may include: forming core transistors with drains on the semiconductor wafer; forming low voltage threshold transistors with drains on the semiconductor wafer; forming input output transistors with drains on the semiconductor wafer; forming a first photoresist mask layer over the low voltage and the input output transistors; doping the drains of the core transistors, wherein the doping is a medium doping; forming a spacing layer over the core, low voltage and input output transistors; forming a second photoresist mask layer over the input output transistors; doping the drains of the core and the low voltage threshold transistors, wherein the doping is a medium doping; forming a third photoresist mask layer over the core and the low voltage transistors; and doping the drains of the input output transistors, wherein the doping is a medium doping.

[0008] Therefore, in accordance with the previous summary, objects, features and advantages of the present disclosure will become apparent to one skilled in the art from the subsequent description and the appended claims taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Fig. 1 is a diagram of the baseline process for low voltage threshold devices;

[00010] Fig. 2 is a diagram of a streamlined method of processing low voltage threshold devices;

[00011] Fig. 3 is a diagram of a method of processing low voltage threshold devices for optimum performance; and

[00012] Fig. 4 is a diagram of a streamlined method of processing low voltage threshold devices.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0010] The present disclosure is described by the embodiments given below. It is understood, however, that the embodiments below are not necessarily limitations to the present disclosure, but are used to describe a typical implementation of the invention.

[0011] The conventional method of making a low voltage threshold (vt) transistor within a device is illustrated by fig. 1. A core transistor 100, a low vt transistor 102, and an input/output transistor 104 are shown at three different process steps. Each transistor is shown with a gate and drains on both sides of the gate. The first process step shown is the core medium doped drain (MDD) step to dope the exposed drains. Before this step, a spacer layer 112, 114, and 116 was formed on top of each transistor 100, 102 and 104. At this step, a first mask layer 106 is formed on top of the low vt 102 and the input/output transistor 104. The first mask allows dopant to reach only the drains of the core transistor 100 and prohibits any from reaching the drains of the low vt 102 and the input/output transistor 104.

[0012] The next step shown is the low vt MDD. In this step, a second mask layer 108 is formed on top of the input/output transistor 104. This second mask layer 108 allows dopant to reach the drains of the core 100 and the low vt 102 transistors, and prohibits the dopant from reaching the drains of the input/output transistor 104.

[0013] The next step shown is the input/output MDD. In this step, a third mask layer 110 is formed on top of the core 100 and the low vt 102 transistors. This third mask layer 110 allows dopant to reach the drains of the only the input/output 104 transistors, and prohibits the dopant from reaching the drains of the core 100 and the low vt 102 transistors.

[0014] A first embodiment of the present invention is illustrated in fig. 2. In this embodiment, by redesigning the masking layers, a process step can be eliminated thereby producing a significant cost savings for each device. The first process step shown is a modified core medium doped drain (MDD) step. Before this step, a spacer layer 112, 114, and 116 was formed on top of each transistor 100, 102 and 104. At this step, a first mask layer 120 is formed on top of the low vt 102. The first mask allows dopant to reach the drains of the core 100 and the input/output 104 transistors and prohibits any from reaching the drains of the low vt 102.

[0015] The next step shown is the low vt MDD. In this step, a second mask layer 108 is formed on top of the input/output transistor 104. This second mask layer 108 allows dopant to reach the drains of the core 100 and the low vt 102 transistors, and prohibits the dopant from reaching the drains of the input/output transistor 104.

[0016] This design of the masking layers and process steps provides the same amount of dopant in each drain as the conventional design, but eliminates a step and thus provides a significant cost savings for each device.

[0017] A second embodiment is illustrated in fig. 3. Again, a core transistor 100, a low vt transistor 102, and an input/output transistor 104 are shown at three different process steps. The first process step shown is the core MDD step. However, unlike the convention design, the spacer layer is not formed before the core MDD step. At this step, a first mask layer 106 is formed on top of the low vt 102 and the input/output transistor 104. The first mask allows dopant to reach only the drains of the core transistor 100 and prohibits any from reaching the

drains of the low vt 102 and the input/output transistor 104. After the doping, the spacer layer 112, 114, and 116 is formed on top of each transistor 100, 102 and 104.

[0018] The next step shown is the low vt MDD. In this step, a second mask layer 108 is formed on top of the input/output transistor 104. This second mask layer 108 allows dopant to reach the drains of the core 100 and the low vt 102 transistors, and prohibits the dopant from reaching the drains of the input/output transistor 104.

[0019] The next step shown is the input/output MDD. In this step, a third mask layer 110 is formed on top of the core 100 and the low vt 102 transistors. This third mask layer 110 allows dopant to reach the drains of the only the input/output 104 transistors, and prohibits the dopant from reaching the drains of the core 100 and the low vt 102 transistors. The new design of the second embodiment results in an optimization of performance of the transistors.

[0020] A third embodiment of the present invention is illustrated in fig. 4. In this embodiment, by another redesign of the masking layers, a process step can be eliminated thereby producing a significant cost savings for each device. The first process step shown is a modified core MDD step. Before this step, a spacer layer 112, 114, and 116 was formed on top of each transistor 100, 102 and 104. At this step, a first mask layer 400 and 402 is formed on top of the low vt 102 and the IO transistor 104, respectively. The first mask allows dopant to reach the drains of the core 100 transistor and prohibits any from reaching the drains of the low vt 102 and the IO transistor 104.

[0021] The next step shown is the low vt MDD. In this step, a mask layer is not formed on top of any of the transistors. The lack of mask layer allows dopant to reach the drains of the core 100, the low vt 102 and the IO 104 transistors.

[0022] This design of the masking layers and process steps also provides the same amount of dopant in each drain as the conventional design, but eliminates a step and thus provides a significant cost savings for each device.

[0023] It is understood that several modifications, changes and substitutions are intended in the foregoing disclosure and in some instances some features of the invention will be employed without a corresponding use of other features. Specifically, although the embodiments illustrate

only one transistor for the core, low vt and the input/output sections, it is understood that each transistor is only illustrative and can actually represent many transistors. In addition, these embodiments, the core section represents most of the electrical devices towards the center of the semiconductor wafer. Accordingly, it is appropriate that the appended claims be construed broadly and in a manner consistent with the scope of the invention.